

## CLAIMS

What is claimed is:

Sub 1  
a1 1. ~~An interface to transfer data directly between a memory control hub (MCH) and~~  
2 a input/output control hub (ICH) within a computer system, comprising:  
3 a data signal path to transmit data in packets via split transactions; and  
4 a set of command signals, wherein said interface provides a point-to-point  
5 connection between said MCH and said ICH, exclusive of an external bus  
6 ~~connected directly to the interface.~~

Sub 1  
D1 1 2. The interface of claim 1, wherein said MCH and said ICH within said computer  
2 system are components within a chipset.

1 3. ~~The interface of claim 1, wherein a first transaction is initiated on said interface~~  
2 ~~with a request packet, subsequent to arbitration for ownership of said interface.~~

Sub 1  
D2 1 4. ~~The interface of claim 3, wherein said request packet includes a transaction~~  
2 ~~descriptor.~~

1 5. The interface of claim 3, wherein a completion packet is transmitted on said  
2 interface in response to said request packet of said first transaction.

1 6. The interface of claim 3, wherein said request packet includes transaction  
2 descriptor and said completion packet includes a corresponding transaction descriptor.

1 7. The interface of claim 5, wherein a request packet for a second transaction can be  
2 transmitted across said interface prior to transmitting said completion packet in  
3 response to the request packet of said first transaction.

1 8. ~~The interface of claim 3, wherein said data signal path is scalable.~~

1 9. The interface of claim 8, wherein packets are transmitted across said data signal  
2 path via a source synchronous clock mode.

1 10. The interface of claim 9, wherein said interface includes a set of bi-directional  
2 data signals, a first and second source synchronous strobe signal, a unidirectional  
3 arbitration signal, and a bi-directional stop signal.

1 11. The interface of claim 10, wherein said interface further includes a system reset  
2 signal, a common clock signal, and a voltage reference signal.

1 12. The interface of claim 11, wherein said transaction descriptors identify separate  
2 hubs within a hierarchy of multiple interfaces between at least three hubs.

1 13. The interface of claim 5, wherein said request packet includes a field indicating if  
2 a completion packet is required in response to the respective request packet.

1 14. The interface of claim 3, wherein arbitration between said hubs is symmetric and  
2 distributed.

1 15. The interface of claim 3, wherein a hub is allotted ownership of said interface up  
2 to a predetermined amount of time.

1 16. An interface to transfer data directly between a memory control hub (MCH) and  
2 an input/output control hub (ICH) within a computer system, comprising:

3 ~~a first means for transmitting data between said MCH and said ICH in packets~~  
4 via split transactions; and  
5 a second means for transmitting command signals, wherein said interface  
6 provides a point-to-point connection between said MCH and said ICH, exclusive  
7 of an external bus connected directly to the interface.

1 17. The interface of claim 16, wherein said ICH and said MCH within said computer  
2 system are components within a chipset.

1 18. The interface of claim 17, wherein said interface includes a means for initiating a  
2 first transaction on said interface with a request packet.

502 19. ~~The interface of claim 18, wherein said request packet includes a transaction  
descriptor.~~

502 20. ~~The interface of claim 19, wherein said interface includes means for providing a  
completion packet in response to said request packet of said first transaction.~~

1 21. ~~The interface of claim 18, wherein said request packet includes a transaction  
2 descriptor and said completion packet includes a corresponding transaction descriptor.~~

502 22. ~~The interface of claim 21, wherein said interface includes a means for  
transmitting request packet for a second transaction across said interface prior to  
3 transmitting said completion packet in response to the request packet of said first  
4 transaction.~~

1 23. The interface of claim 22, wherein said first means for transmitting data in  
2 packets via split transactions includes further includes means for scaling a data signal  
3 path.

1 24. The interface of claim 23, wherein said interface includes means for transmitting  
2 packets across said interface via a source synchronous clock mode.

1 25. The interface of claim 21, wherein said transaction descriptors include a means  
2 for identifying separate hubs within a hierarchy of multiple interfaces between three or  
3 more hubs.

1 26. The interface of claim 20, wherein said request packet includes a means for  
2 indicating if a completion packet is required in response to the respective request  
3 packet.

1 27. The interface of claim 26, wherein interface includes a means for arbitrating  
2 between said hubs for ownership of said interface.

1 28. The interface of claim 21, wherein said interface further includes a means for is  
2 allotting ownership of said interface to one of said hubs up to a predetermined amount  
3 of time.

1 29. An interface to transfer data between a memory control hub and an  
2 input/output (I/O) hub of a chipset within a computer system, comprising:  
3 a bi-directional data signal path and a pair of source synchronous strobe signals,  
4 said data signal path transmits data in packets via split transactions, said packets

5 ~~including a request packet and completion packet, said request packet including a~~  
6 transaction descriptor ; and  
7 a set of command signals including unidirectional arbitration signal, a bi-  
8 directional stop signal, a system reset signal, a common clock signal, and a voltage  
9 reference signal, wherein said interface provides a point-to-point connection between  
10 said memory control hub and said I/O hub, exclusive of an external bus connected  
11 directly to the point-to-point connection.

1 30. A computer system comprising  
2 a processor;  
3 a memory control hub (MCH) coupled to said processor;  
4 an input/output control hub (ICH) coupled to said MCH via an interface to  
5 transfer data directly between the MCH and the ICH;  
6 said interface having a data signal path to transmit data in packets via split  
7 transactions, and said interface including a set of command signals, wherein said  
8 interface provides a point-to-point connection between said MCH and said ICH,  
9 exclusive of an external bus connected directly to the point-to-point connection; and  
10 at least one peripheral component coupled to said ICH.

1 31. The computer system of claim 30, wherein said peripheral component is a  
2 Peripheral Component Interconnect (PCI) agent.

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2 32. The computer system of claim 31, wherein said first and second hubs within said  
3 computer system are components within a chipset.

1 ~~33.~~ The computer system of claim 32, wherein a first transaction is initiated on said  
2 interface with a request packet, subsequent to arbitration for ownership of said  
3 interface.

1 34. The computer system of claim 33, wherein said request packet includes a  
2 transaction descriptor.

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1 35. ~~The computer system of claim 33, wherein a completion packet is transmitted on~~  
2 ~~said interface in response to said request packet of said first transaction.~~

1 36. ~~The computer system of claim 35, wherein said request packet includes a~~  
2 ~~transaction descriptor and said completion packet includes a corresponding transaction~~  
3 ~~descriptor.~~

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1 37. ~~The computer system of claim 36, wherein a request packet for a second~~  
2 ~~transaction can be transmitted across said interface prior to transmitting said~~  
3 ~~completion packet in response to the request packet of said first transaction.~~

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1 38. ~~The computer system of claim 36, wherein said data signal path is scalable.~~

1 39. The computer system of claim 38, wherein packets are transmitted across said  
2 data signal path via a source synchronous clock mode.

1 40. The computer system of claim 39, wherein said interface includes a set of bi-  
2 directional data signals, a first and second source synchronous strobe signal, a  
3 unidirectional arbitration signal, and a bi-directional stop signal.

1 41. The computer system of claim 40, wherein said interface further includes a  
2 system reset signal, a common clock signal, and a voltage reference signal.

1 42. The computer system of claim 41, wherein said transaction descriptors identify  
2 separate hubs within a hierarchy of multiple interfaces between at least three hubs.

1 43. The computer system of claim 42, wherein said request packet includes a field  
2 indicating if a completion packet is required in response to the respective request  
3 packet.

1 44. The computer system of claim 43, wherein arbitration between said hubs is  
2 symmetric and distributed.

1 45. The computer system of claim 44, wherein a hub is allotted ownership of said  
2 interface up to a predetermined amount of time.

1 46. The computer system of claim 31, wherein the computer system includes  
2 multiple processors.

1 47. The computer system of claim 31, wherein the computer system further includes a  
2 third hub coupled to said ICH via an interface comprising:  
3 a bi-directional data signal path and a pair of source synchronous strobe signals,  
4 said data signal path transmits data in packets via split transactions, said packets  
5 including a request packet and completion packet, said request packet including a  
6 transaction descriptor ; and

7 a set of command signals including unidirectional arbitration signal, a bi-  
8 directional stop signal, a system reset signal, a common clock signal, and a voltage  
9 reference signal.

1 48. The computer system of claim 31, wherein the processor and the MCH of said  
2 computer system, are integrated on a single semiconductor unit.

1 49. The computer system of claim 31, wherein the MCH and a graphics unit of said  
2 computer system, are integrated on a single semiconductor unit.

1 50. A memory control hub (MCH) comprising:  
2 an interface to transfer data directly to an input/output control hub (ICH) within  
3 a computer system, the interface having a data signal path to transmit data in  
4 packets via split transactions, and a set of command signals, wherein the  
5 interface provides a point-to-point connection between said the MCH and said  
6 ICH, exclusive of an external bus connected directly to the interface.

1 51. The memory control hub of claim 50, wherein said MCH and ICH are  
2 components within a chipset.

1 52. The memory control hub of claim 50, wherein a first transaction is initiated on  
2 said interface with a request packet, subsequent to arbitration for ownership of said  
3 interface.

1 53. The memory control hub of claim 52, wherein said request packet includes a  
2 transaction descriptor.



1 54. The memory control hub of claim 53, wherein a completion packet is transmitted  
2 on said interface in response to said request packet of said first transaction.

1 55. The memory control hub of claim 52, wherein said request packet includes  
2 transaction descriptor and said completion packet includes a corresponding transaction  
3 descriptor.

1 56. The memory control hub of claim 55, wherein a request packet for a second  
2 transaction can be transmitted across said interface prior to transmitting said  
3 completion packet in response to the request packet of said first transaction.

1 57. The memory control hub of claim 56, wherein said data signal path is scalable.

1 59. The memory control hub of claim 57, wherein packets are transmitted across said  
2 data signal path via a source synchronous clock mode.

1 60. The memory control hub of claim 59, wherein said interface includes a set of bi-  
2 directional data signals, a first and second source synchronous strobe signal, a  
3 unidirectional arbitration signal, and a bi-directional stop signal.

1 61. The memory control hub of claim 60, wherein said interface further includes a  
2 system reset signal, a common clock signal, and a voltage reference signal.

1 62. The memory control hub of claim 61, wherein said transaction descriptors  
2 identify separate hubs within a hierarchy of multiple interfaces between at least three  
3 hubs.

1 63. ~~The memory control hub of claim 62, wherein said request packet includes a field~~  
2 ~~indicating if a completion packet is required in response to the respective request~~  
3 ~~packet.~~

1 64. The memory control hub of claim 63, wherein arbitration between said hubs is  
2 symmetric and distributed.

1 65. The memory control hub of claim 64, wherein a hub is allotted ownership of said  
2 interface up to a predetermined amount of time.

1 66. The memory control hub of claim 50, wherein the memory control hub and a  
2 ~~processor are integrated on a single semiconductor unit.~~

1 67. The memory control hub of claim 50, wherein the memory control hub and a  
2 graphics unit are integrated on a single semiconductor unit.